IN THE SPECIFICATION

Page 5, replace the first full paragraph with the following:

FIG. 2 shows an embodiment of instruction memory system 12 for use with instructions of different length. Instruction memory system 12 contains a plurality of memory units 20, 22, a multiplexer 24, ~~a clock unit 26~~ and clock gating circuits 28a,b, and is coupled to a clock unit 26. An address input 23 of instruction memory system 12 is coupled at least partly to address the memory units 20, 22. A first one of the memory units 20 has a word size that is larger than the word size of a second one of the memory units 22. (Symbolically a first memory unit 20 is shown wider than second memory unit 22, to indicate the first memory units' wider instruction word size, whereas second memory unit 22 is shown higher than first memory unit 20 to indicate that second memory contains locations for a greater number of instruction words). Instruction outputs of memory units 20, 22 are coupled to inputs of multiplexer 24, the instruction output of the second one of the memory units 22 being coupled to the input of the multiplexer 24 in combination with default input 29 (which supplies for example no-operation instructions). An output of multiplexer 24 is coupled to instruction execution unit 14 (not shown). Clock unit 26 is coupled to clock inputs of memory units 20, 22, each via a respective one of the clock gating circuit 28a,b. An output of address range detector 16 is coupled to an input 11 of instruction memory system 12 that is coupled to a control input of multiplexer 24 and to disable inputs of clock gating circuits 28a,b.

Page 11, replace the first full paragraph with the following:

FIG. 5 shows a flow chart for programming the processing apparatus of FIG. 1. In a first step 51 of the flow chart a program is compiled and instructions are generated for executing the program. In a second step 52, the position of the inner loop (or loops) in the program are determined. This may be done by automatic code inspection, or by profiling (that is, counting the number of times different instructions are executed during trial execution for typical input data). In a third step, 53 the instruction words are formed, the

instruction words in the inner loops being optimised, for example by using known techniques such as (partial) loop unrolling, or by providing instructions for special purpose functional units. In a fourth step 54 the instruction words are loaded into instruction memory system 12 so that the instruction words in the inner loop are stored at memory locations with instruction addresses in the range where instruction memory system stores wider instruction words, or where instruction execution unit selects to execute more instructions from the instruction word in parallel. Alternatively, the bounds of the range are set according to the locations where the instruction words of the inner loop have been loaded.